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Review

A review on quality factor enhanced on-chip microwave planar resonators

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ABSTRACT

This paper reviews microwave on-chip resonators with emphasis on quality-factor (*Q*-factor), and techniques enhancing *Q*-factor. The review discusses both planar microstrip and waveguide structures, with the integration of the latter emerging as a substitute for the bulky and expensive non-planar waveguides. Despite their huge *Q*-factor the conventional waveguide does not support integration and miniaturisation. While the microstrips support miniaturisation and mass fabrication at low-cost, they are limited by low *Q*-factor due to high conductor and substrate losses. A study of *Q*-factor enhancing techniques for on-chip devices is presented, with an introduction of integrated waveguide structures. In addition, a summary of transitions between on-chip planar microstrips and planar waveguides is presented.

Contents

1. Introduction

The demand for portable and efficient wireless devices prompts the need for integrated circuits of high quality (*Q*-factor), for high level integration at high frequencies. These circuits include planar microstrip resonators [1] and planar integrated waveguide [2]. Despite the advantage of small circuit size and high integration density [3,4], planar resonators suffer huge transmission loss due to conductor and substrate losses [5,6]. However their application to microwave and millimetre-wave frequency is unavoidable, thus instigating research in loss reduction mechanisms to improve *Q*-factor and circuit performance. Consequently, various loss reduc-

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tion [7] and Q-enhancement [8] methods were presented in previous works and some of those techniques are discussed in subsequent sections of this paper.

1.1. Overview of microstrips

Integrated transmission lines (microstrips) are the most fundamental elements in the design of low-cost miniaturized microwave circuits [9] such as filters and antennas. For many years microstrip circuits were used for filtering application at lower frequencies in the radio frequency (RF) range. These circuits gained popularity with the advantage of low-cost, easy fabrication, planar nature and ability to integrate with solid-state devices. Even with the above mentioned advantages, the circuit experience excessive conductive and magnetically induced losses [10]. While radiation and dielectric losses are also significant, ohmic losses due to lossy substrate and metal traces are the two main contributors to the overall losses of the circuit. This leads to very low Q-factor for on-chip elements compared to their off-chip counterparts. Enormous advancement in research on the performance trends, modelling and design [11–14], optimisation and Q-factor enhancement methods of microstrip circuits and substantial results are reported [8,15–17] for various RF applications. Some of these techniques are introduce and discuss in Section 2 of this manuscript.

1.2. Overview of substrate integrated waveguide

Substrate Integrated Waveguide (SIW) [18–21] technology emerged in the last two decades as an alternate design of resonant structures for microwave and millimetre-wave applications. These are substrate integrated circuits (SICs) [22] made-up of double rows of conducting slots immersed in a dielectric substrate that connects two plates on either side of the substrate. Like the microstrip structures, they are affected by conductor, radiation and dielectric losses [23] limiting their performance. Despite losses related to conductor and substrate materials, the SIWs possess the characteristics of a rectangular waveguide such as high Q-factor and low radiation loss with an extra advantage of reduced size by a factor of $\varepsilon^{1/2}$ [24] to the original size. In addition, the unloaded Q-factor of SIWs is much greater than that of microstrip circuit [19], therefore these are fundamental components for high frequency ICs. Some SICs are a combination of SIW and a microstrip in what is normally as a hybrid integration [25]. The application of the SICs to high frequency devices provide an alternate solution to high performing circuits with complementary advantages of microstrips and waveguide circuits [26]. Several publications introduce and discuss these structures, and a summary is presented on Section 3 of this manuscript.

1.3. Quality-factor

As a figure of merit, Q-factor determines the performance of any resonant structure. It is defined as the ratio of energy stored to the total energy lost per cycle for a sinusoidal excitation. Q-factor is described by (1) as in [27],

$$Q = 2\pi \frac{Energy\ stored}{(energy\ lost\ per\ cycle)} \tag{1a}$$

$$= 2\pi \frac{E_{mag,max} - E_{elec,max}}{P_{avg}} \tag{1b}$$

Where $E_{mag,max}$ and $E_{elec,max}$ are the maximum magnetic and electric energy respectively, and P_{avg} is the average power dissipated. Eqs. (1a) and (1b) show that Q-factor is highly dependent on the amount of energy lost per cycle. An increase in energy loss results in low Q-factor prompting the need for Q-enhancement mechanism. Despite several Q-enhancing techniques reported [2,9,25,28,29] it is difficult to achieve high Q-factor in planar structures. An investigation on the state-of-the-art progress in Q-enhancement is discussed in this paper.

The paper is structured as follows: Section 1 – provides a general introduction to on-chip and substrate integrated resonators, Section 2 – analyses on-chip microstrip resonator and Q-enhancement methods, Section 3 – analyses substrate integrated waveguide with Q-factor consideration, Section 4 – reviews hybrid integration of conventional planar structures to non-planar structures on a single substrate, and Section 5 – reviews substrate material properties and effect on resonator performance.

2. Microstrip analysis

In its simplest form, a microstrip resonator consists of two metal conductors separated by a dielectric substrate as illustrated in Fig. 1. The suspended metal trace on the substrate is a strip-line whereas the underneath metal plate is a ground plane.

Microstrip lines are used to develop inductors in various shapes as presented by Fig. 2. An inductor with least number of sides is square spiral [31,32], while the one with infinite number of sides

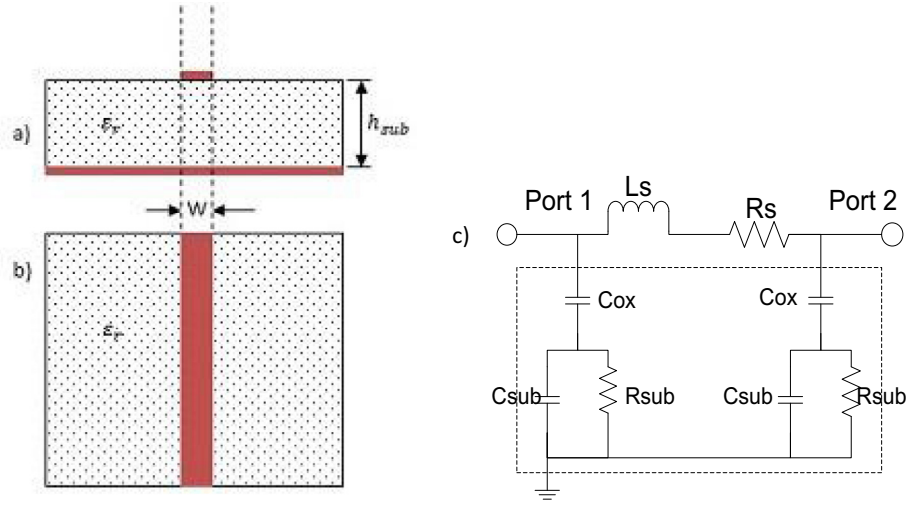

Fig. 1. Microstrip geometry a) side-view, b) top-view, and c) equivalent lump circuit [30].

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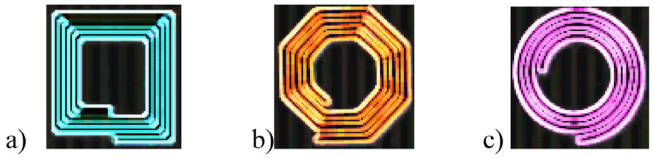

Fig. 2. layout of spiral inductor a) square, b) octagonal, and c) circular [37].

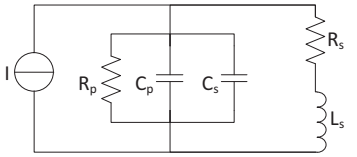

Fig. 3. Equivalent of a terminal grounded inductor for modelling the Q-factor [40].

is a circular spiral [33–35]. The former has a high inductance value but low Q-factor due to current crowding effect [36] at the sharp corners, and the latter has a lower inductance value but higher Q-factor.

Shi et al. [8] reported an effective way of improving Q-factor on an on-chip spiral inductor. They focused on a circular spiral, the best possible layout structure in the family of planar spiral inductors. These spiral uses less chip area while making use of large chunks of metal conductors which reduces the series resistance [30]. Despite better Q-factor due to less series resistance, the spiral popularity is very low because it is difficult to layout compared to other shapes. This makes the square spiral the more popular because it is the easy to layout. Talwalkar et al. analysed and synthesised on-chip inductor and reported [38] several limitations on the inductors. They cited penetration of electric and magnetic field into the substrate as factors limiting the spiral performance. In addition, current redistribution in the microstrip and current redistribution due to adjacent conductors also diminish the spiral performance. While both the spiral and substrate parameters are important for modelling Q-factor, at low frequencies the substrate-loss factor (F_S) and the self-resonance factor (F_R) [39] are almost equal to unity. Therefore only the magnetic energy stored by the inductor is important for Q-factor evaluation. This implies the shunt branch in the circuit of Fig. 3 could be ignored for Q-factor formulation thus leading to (2).

$$Q = \frac{\omega L_s}{R_s} \tag{2}$$

where ω is the angular frequency in rads, L_s is the series inductance and R_s is the series resistance of the inductor. An increase in frequency results in significant reduction in Q-factor due to F_S and F_R leading to (3) as in [39–41].

$$Q = \frac{\omega L_s}{R_s}\left[\frac{R_p}{R_p + \left[\left(\frac{\omega L_s}{R_s}\right)^2 + 1\right]R_s}\right]\left[1 - \frac{R_s^2(C_s + C_p)}{L_s} - \omega^2 L_s(C_s + C_p)\right] \tag{3}$$

where the middle term represents the F_S and the last term represents the F_R of the circuit. Symbols C_p and R_p are the coupling capacitance and coupling resistance respectively, and C_s is the series capacitance between the metal lines [40]. The limiting factor in microstrip Q-factor is R_s of metallisation. Other factors contributing to this limitations are conductive substrate losses normally from 1 to 10 Ω-cm. These are more common in the silicon based substrates because of the conductivity nature of silicon [42]. The main cause of substrate loss is the inductive coupling normally caused by the magnetic fields entering the substrate, inducing some eddy current [40,43–46]. These currents increase the substrate losses leading to reduced spiral performance and Q-factor, therefore several Q-factor enhancement techniques were introduced to compensate for the energy losses and Q-improvement. Some of these techniques are as follows.

2.1. Layout Optimisation

The layout optimisation [47] technique optimises the width of the metal trace for each turn by varying the metal width of the spiral inductor. This method was introduced in the past two decades after Craninckx and Steyaert [48] discovered that the series resistance in a spiral inductor is caused by the arrangement of the inner turns, highlighting the small radius as the main contributor to the ohmic losses at high frequency. According to their study, the induction of electric field at the centre of the spiral generates eddy currents in the inner turns. Consequently, the generation of eddy currents results in non-uniformity of current distribution thus causing high series resistance in the inner turns. Lopez-Villegas et al. used this technique to design a square spiral inductor in a silicon-based multichip technology complemented with a silicon micromachining post-processing and managed to observe a Q-factor improvement of 60% at a frequency of 3.5 GHz [47]. Recently, Pei et al. applied the same technique on a square spiral with non-uniform strip width and non-uniform winding spacing obtaining an improvement of 42.86% [27]. It is clear that the physical structure and layout of microstrip inductor plays a very important role in Q-factor enhancement.

2.2. Patterned ground shield (PGS)

Patterned ground shield (PGS) [39] is one of the various techniques discovered to enhance performance of on-chip spirals for silicon-based RFICs [8]. The technique shorts the electric field to the ground plane. It is patterned with slots orthogonal to the spiral inductor to eliminate the induced current loop by cutting off the current path [39]. These slots are significantly narrower to prevent the vertical electric field from entering the silicon substrate underneath. Pokharel and Liu in Ref. [49] proposed a low loss, high selective on-chip bandpass filter employing the improved open loop resonator with folded structure and the PGS. Similarly, Liao et al. in Ref. [8] demonstrated that a proper PGS can effectively compensate for the degradation of the Q-factor, thus improving the Q-factor of the inductor. The PGS technique effectively reduces the substrate coupling resistance [14]. Tao Zheng et al. used this technique and obtained a high Q-value on a low resistivity silicon wafer [50].

2.3. Differentially excitation

Differential circuits [51] are commonly used to develop monolithic transceiver design due to their robustness and very high noise rejection properties [52]. While this topologies are used in ICs, they are practically used to excite spiral inductors by connecting the source directly to the two terminals of the spiral inductor [42]. The differential excitation method reduces eddy currents circulation by a significant 30–50% [52] and limit the electrically coupled currents from occurring in the substrate by 50% [51]. A three turn spiral inductor with an outer diameter of 220 μm, spiral width of 16 μm, and coil spacing of 2 μm was fabricated in a 0.35 μm single-poly, four metal CMOS process [30]. This design yielded a differential Q-factor of 3.1, 50% greater than Q-factor of the single-ended excitation at 2.5 GHz.

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Table 1
Summary of Q-improvement techniques reported in literature.

Method	Original-Q	Final-Q	Improvement	Other References
Layout optimisation	17@1.5 GHz	40@3.5 GHz [47]	Over 60%	[11,17,58,59]
Differential excitation	6.6@1.6 GHz	9.3@2.5 GHz [52]	Over 50%	[30,42,51]
Negative resistance	3.84@3.1 GHz	4.73@3.7 GHz [60]	Over 20%	[43,53,54]
PGS	5.08@2.0 GHz	6.76@2.0 GHz[39]	Over 30%	[8,39,61]

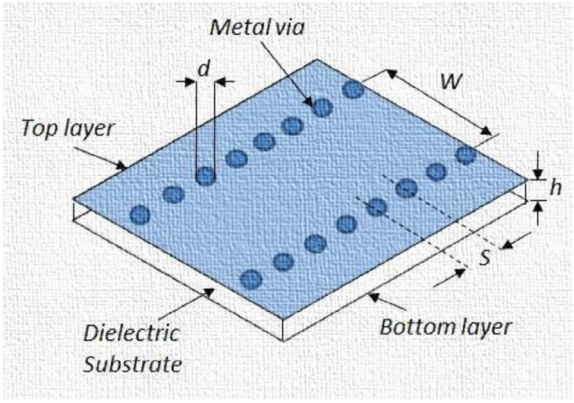

Fig. 4. Geometry of a substrate integrated waveguide [76].

2.4. Negative resistance

The negative resistance is a loss compensation mechanism that introduces a negative resistance of magnitude $-R_s$ to reduce the dominant ohmic losses in the spiral traces. In this case, the negative resistor is placed in series with $+R_s$ to cancel out or reduce the amount of losses caused by $+R_s$ [43]. This approach was reported by [53–57], stating that the Q-factor is enhanced by using an active negative resistance placed in series to the lossy microstrip inductor. In addition [57], states that a tapped-inductor feedback techniques results in a higher Q-factor by producing a negative feedback. This compensates for the conductor losses related to Q-factor, thus improving the total Q-factor of the resonating structure (Table 1).

3. SIW analysis

The introduction of SIWs in Refs. [18–24,62–74] presents the most promising resonant structures with high Q-factor, low-loss, mass-fabrication and integration on a single substrate. This technique allows for a waveguide size reduction with a factor of $\varepsilon^{1/2}$ [75] to the conventional rectangular waveguide. Although they possess high-Q and low-loss over on-chip spirals, SIW structures are still large to integrate in front-end devices, hence more research on size reduction is still necessary. Fig. 4 illustrates a physical geometry of these structures with the metal vias representing the slots connecting the two metal plates on either side of the structure.

The rectangular characteristics realised by the metal vias represents the rectangular waveguide effective width (W_{eff}) that exhibit modal propagation properties corresponding to the considered SIW. Most commonly, (4) and (5) proposed in Refs. [23,70,77] are used to calculate the effective width and length of the waveguide.

$$W_{eff} = W - \frac{d^2}{0.95s} \tag{4}$$

$$L_{eff} = L - \frac{d^2}{0.95s} \tag{5}$$

where d is the diameter of each via, W and L are the physical width and length of the waveguide while s is the centre to centre distance between two adjacent vias.

3.1. Losses and Q-factor of SIW

SIW losses are divided into three main contributors, the conductor, dielectric and radiation losses. Conductor losses exhibited by these structures are due to the finite conductivity of metal layers and vias while dielectric losses are due to loss tangent of the dielectric substrate. In addition, radiation losses, usually very minimal are due to the gaps in the SIW structure along the walls [72]. Since these are very minimal, they could be ignored in the calculation of the total Q-factor (Q_T) given by (6) as in Ref. [23].

$$\frac{1}{Q_T} = \frac{1}{Q_D} + \frac{1}{Q_C} \tag{6}$$

where,

$$Q_D = \frac{1}{\tan\delta} \tag{7}$$

$$Q_C = \frac{\lambda_r}{\delta}\beta \tag{8}$$

Symbol β represents a shape factor of the SIW for resonance in TE_{101} mode defined by,

$$\beta = \frac{W_{eff}L_{eff}^{h}}{2} \frac{\left(\frac{1}{W_{eff}^2} + \frac{1}{h^2}\right)^{3/2}}{\frac{h}{W_{eff}^2}\left(W_{eff} + 2L_{eff} + \frac{W_{eff}}{h^2}(h + 2L_{eff})\right)} \tag{9}$$

where, W_{eff}, L_{eff} and h are the width, length and height of the SIW respectively. The field distribution similarities of SIW and rectangular waveguide mean that the procedure for calculating conductor loss attenuation factor is the same. Therefore, the expression derived from the traditional rectangular waveguide is used to calculate the attenuation factor α_C of the SIW, thus W_{eff} in (4) above is the equivalent width of a rectangular waveguide,

$$\alpha_C(f) = \frac{\sqrt{\pi f \varepsilon_0 \varepsilon_R}}{h\sqrt{\sigma_C}} \frac{1 + 2\left(\frac{f_0}{f}\right)^2 h/w_{eff}}{\sqrt{1 - \left(\frac{f_0}{f}\right)^2}} \tag{10}$$

$$\alpha_D(f) = \frac{\pi f \sqrt{\varepsilon_r}}{c\sqrt{1 - \left(\frac{f_0}{f}\right)^2}} \tan(\delta) \tag{11}$$

$$\alpha_R = \frac{\frac{1}{w}\left(\frac{d}{w}\right)^{2.84}\left(\frac{s}{d} - 1\right)^{6.28}}{4.85\sqrt{\left(\frac{2w}{\lambda}\right)^2 - 1}}. \tag{12}$$

Eq. (11) represents the attenuation factor due to conductor losses, where h is substrate thickness, ε_0 is the dielectric permittivity of space, ε_R is the dielectric permittivity of substrate, f_o is the cut-off frequency of the SIW, f is the frequency of operation and σ_C is the conductivity of metal [78]. Eq. (12) represents the attenuation factor due to the dielectric losses, where c is the speed of

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light. Attenuation due to radiation loss is represented by (13), where λ is the wavelength in the dielectric at a particular frequency of operation. From (11) to (13) the attenuation constant [78–80] of the SIW is calculated as,

$$\alpha_O = \alpha_C + \alpha_D + \alpha_R, \quad (13)$$

3.2. Enhanced Q-factor of SIWs

Traditionally, rectangular waveguide has very high Q-factor of over 10,000. However their integration to planar form presents some losses due to size reduction, and losses induced by the dielectric material. Despite these limitations, modification of geometrical parameters such as substrate thickness, via diameter and inter-via spacing minimizes the losses, and thus improve the quality factor of the SIW. As stated in Ref. [23], Q-factor of SIW is directly proportional to the substrate thickness, and a high-Q is achieved with a thicker substrate. Nonetheless, it is not comparable to the Q-factor of a rectangular waveguide at high frequencies, with the microstrip having the lowest of them all.

An enhanced total Q-factor of an SIW circuit requires improved individual Q-factors related to dielectric losses (Q_D) and conductor losses (Q_C). A modified SIW (MSIW) in Ref. [68] uses an air-cut to reduce and increase the dielectric loss, and Q_D respectively. However, the proposed structure suffers energy losses due to conductor losses leading to low Q_C. This method was also applied in Ref. [7] with the central section of the SIW removed leaving an air-fill between the two rows of vias. Ghiotto et al. reported on an air-filled SIW in Refs. [80,81]. They demonstrated that the air-filled SIW outperforms a dielectric-filled SIW in transmission loss reduction and Q-factor improvement. Recently, Tong et al. proposed in Ref. [79] an SIW in a very thin glass substrate with Trough-Package-Vias (TPVs). The results showed a significant reduction in transmission losses making glass an ideal package substrate at very high frequencies. Despite not reporting on the Q-factor value, it was evident that glass reduces field strength on the substrate, and since Q-factor is highly dependent on the amount of electric and magnetic fields, the assumption is that, their design offered high-Q due to reduced field strength.

4. Hybrid integration

Hybrid integration [81–83] is a technique of microwave circuit integration, in which non-planar circuits are integrated with planar circuits on the same substrate. This technique combines the advantages of conventional microstrip and non-planar structures such as rectangular waveguide [82] to build a high performing SIC. The complementary advantages are merged within a combined fabrication platform, in which non-planar structures are synthesized and converted to planar form [3,22,25]. Several developments are reported in literature, in which transitions between planar structures and non-planar structure or vice versa were implemented. The most common transition in recent years is the transition of conventional planar structures to the non-planar structures [2,6,71,84,85]. Dominic Deslandes and Ke Wu [2] earlier developed a new planar platform combining the integration of microstrip line and rectangular waveguides on a single substrate using a tapered microstrip line. Accordingly, the 3D mounting structures are a required to design an integrated planar rectangular waveguide possessing high Q-factor. The transition basically consist of a tapered microstrip line interconnected to microstrip and waveguide both of different widths as illustrated in Fig. 5 below [6].

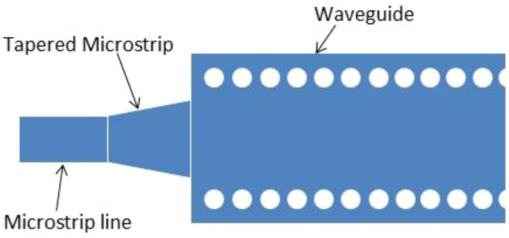

Fig. 5. Microstrip to waveguide.

Wang et al. designed two half-mode SIW filters in Ref. [84], both of which a microstrip-HMSIW transition was used. They realised a three pole and five pole filters with low insertion loss and good selectivity. Compared to the conventional SIW, their proposal showed more improvement in terms of size miniaturisation and space between the passband and spurious passband. Lately, Belenguer et al. developed a novel empty substrate integrated waveguide (ESIW) reported in Ref. [85]. Their proposal yield better performance with low-loss and improved-Q at a frequency ranging from 11 to 19.5 GHz.

5. Effect of substrate material on resonator performance

Substrate material plays a vital role in the overall performance of an integrated circuit. The most important parameters to consider when designing a substrate integrated device are the substrate's resistivity and dielectric loss (Table 2). This is due to the fact that materials with high resistivity and low dielectric loss tend to enhance performance of resonant circuits [86]. The evolution of substrate technology started from as far as ceramic technology, followed by organic materials and most recently silicon. Lately, more interest in glass as a substrate for 2.5D/3D application [87–89]. Glass proved to provide better electrical performance compared to silicon. Despite it being an insulator, and edged by silicon in terms of conductivity, glass provides reliability performance as a result of possibility to adjust its thermal properties [87]. Glass substrate is reported in Refs. [88,90–94]. Several other materials such as low temperature co-fired ceramic (LTCC) are regarded suitable for various applications where metal with excellent conductivity such as gold and silver are used. LTCC have a lower dielectric constant as well as low insertion loss. This makes it an ideal substrate for RF and microwave application. Silicon substrate [39,41,86,95] is the most commonly used because of its excellent thermal conductivity. Trott and Shorey studied the mechanical properties of glass and silicon, and they reported that a thinned silicon substrate for integrated circuits has become a common process to meet the packaging form factor required by consumer applications [96]. Nonetheless, the thinned silicon substrate is difficult to handle,

Table 2
Properties of various substrate materials used for MIC design.

Ref.	Material	Dielectric value	Loss tangent	Thermal conductivity
[97]	FR4	4.5	0.025	0.25–0.5 W/m-K
[97]	Duroid 6010.2 LM™	10.2	0.0023	0.860 W/m-K
[98]	Glass	4.5–5.5	0.02–0.03	0.2 W/m-K
[98]	HTCC	8.5–10	0.0005–0.0025	−25 W/m-K

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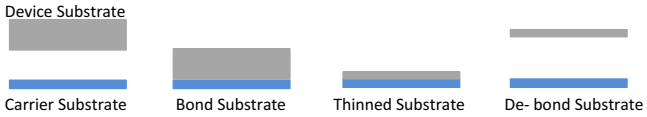

Fig. 6. Temporary bonded carrier for silicon substrate thinning process [96].

thus requiring the use of a carrier substrate bonded temporarily as an aid to handling. The procedure for thinning the substrate is illustrated in Fig. 6.

6. Conclusion

While SIWs offer high-*Q* at higher frequency, larger dimensions proves to be the limiting factor in production of miniaturised RF applications. With the demand for very small and portable RF gadgets, the popularity of spiral inductors continues to increases. The advantage of low-cost, easy fabrication and small size make them the most suitable components for most RF applications. Despite huge transmission losses, spiral inductors are widely used and their application has penetrated the millimetre wave band. Their application at very high millimetre-wave frequency grows with huge attraction from markets in the 60-GHz wireless local area network, and 77-GHz collision avoidance automotive radar [99]. It is therefore important to investigate more on these RF components, to improve the overall performance and *Q*-factor at higher frequencies.

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